1. A method for making a silicon-germanium layer on a substrate for a base of a bipolar transistor comprising the steps of:

providing said substrate having a shallow trench isolation region surrounding a device area with a first type dopant;

depositing an insulating layer and a polysilicon layer on said substrate, and patterning to form an opening over said device area;

forming a blanket seed layer on said substrate and said polysilicon layer at a first temperature;

forming said silicon-germanium layer in-situ doped with a second type dopant, and forming a silicon cap layer on said blanket seed layer at a second temperature;

patterning said silicon cap layer, said silicon-germanium layer, said seed layer, and said polysilicon layer to said insulating layer to form a silicon-germanium base over said device area.

2. The method of claim 1, wherein said substrate is a single-crystal silicon wafer having a crystallographic orientation of <100>.

3. The method of claim 1, wherein said first type dopant is phosphorus.

4. The method of claim 1, wherein said insulating layer is silicon oxide deposited by chemical vapor deposition to a thickness of between about 300 and 800 Angstroms.

5. The method of claim 1, wherein said polysilicon layer is deposited by chemical vapor deposition to a thickness of between about 300 and 800 Angstroms, and is doped with boron to a concentration of between about 1.0 E 18 and 1.0 E 20 atoms/cm^3.

6. The method of claim 1, wherein said blanket seed layer is silicon formed by epitaxial deposition on said device area to a thickness of between about 100 and 300 Angstroms.

7. The method of claim 1, wherein said first temperature is in a range of between about 600 and 750°C, and said seed layer is deposited for a time of between about 200 and 600 seconds.

8. The method of claim 1, wherein said silicon-germanium layer is formed to a thickness of between

about 200 and 1000 Angstroms, and wherein said second temperature is in a range of about 50°C lower than said first temperature.

9. The method of claim 1, wherein said silicon-germanium layer doped with said second type dopant is in-situ doped with boron to a concentration of between about 1.0 E 18 and 1.0 E 20 atoms/cm^3.

10. The method of claim 1, wherein said silicon-germanium layer has a germanium content of between about 10 and 20 atomic percent.

11. The method of claim 1, wherein said silicon-germanium layer is formed by molecular-beam epitaxy.

12. A method for making a silicon-germanium layer on a substrate for a base of an NPN bipolar transistor comprising the steps of:

providing said substrate having a subcollector doped with phosphorus;

forming shallow trench isolation regions over said subcollector and surrounding device areas for said base;

depositing an insulating layer and a polysilicon layer on said substrate;

forming openings in said polysilicon layer and said insulating layer over each of said device areas and said openings partially extending over said shallow trench isolation regions;

forming a blanket seed layer on said substrate to form an epitaxial layer over said device areas, said seed layer formed at a first temperature to reduce the grain size of said seed layer over said shallow trench isolation regions;

forming said silicon-germanium layer in-situ doped with boron, and forming a silicon cap layer on said blanket seed layer at a second temperature to minimize profile of said boron;

patterning said silicon cap layer, said silicon-germanium layer, said seed layer, and said polysilicon layer to said insulating layer to form a silicon-germanium base over said device areas extending over said shallow trench isolation regions to provide areas for base contacts.

13. The method of claim 12, wherein said substrate is a single-crystal silicon wafer having a crystallographic orientation of <100>.

14. The method of claim 12, wherein said subcollector is doped with phosphorus to a concentration of between

about 1.0 E 16 and 1.0 E 17 atoms/cm^3.

15. The method of claim 12, wherein said insulating layer is silicon oxide deposited by chemical vapor deposition to a thickness of between about 300 and 800 Angstroms.

16. The method of claim 12, wherein said polysilicon layer is deposited by chemical vapor deposition to a thickness of between about 300 and 800 Angstroms, and is doped with boron to a concentration of between about 1.0 E 18 and 1.0 E 20 atoms/cm^3.

17. The method of claim 12, wherein said blanket seed layer is silicon formed by epitaxial deposition on said device areas to a thickness of between about 100 and 300 Angstroms.

18. The method of claim 12, wherein said first temperature is in a range of between about 600 and 750 $^\circ$C, and said seed layer is deposited for a time of between about 200 and 600 seconds.

19. The method of claim 12, wherein said silicon-germanium layer is formed to a thickness of between about 200 and 1000 Angstroms, and wherein said

second temperature is in a range of about 50°C lower than said first temperature.

20. The method of claim 12, wherein said silicon-germanium layer is in-situ doped with boron to a concentration of between about 1.0 E 18 and 1.0 E 20 atoms/cm^3.

21. The method of claim 12, wherein said silicon-germanium layer has a germanium content of between about 10 and 20 atomic percent.

22. The method of claim 12, wherein said silicon-germanium layer is formed by molecular-beam epitaxy.

23. The method of claim 12, wherein said silicon-germanium layer is formed by chemical-vapor deposition.